

REMARKS

Claims 1-20 are pending in this application. By this Amendment, claim 1 is amended to more fully define the structure of the optical interconnection circuit over the teachings of the cited art, as discussed more fully below.

No new matter is added by this Amendment. Support for the amendments to claim 1 may be found in the original specification, for example in the original Figures and at paragraph [0099].

I. Rejections Relying Upon Yoshimura 736

Claims 1-7, 12 and 19-20 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,693,736 (Yoshimura 736). In addition, claims 8-11 and 13-18 were rejected under 35 U.S.C. §103(a) relying upon Yoshimura 736. These rejections are respectfully traversed.

As amended, claim 1 recites an optical interconnection circuit between chips that includes a first micro tile element having a light emitting part provided on the substrate, a second micro tile element having a light receiving part provided on the substrate, and an optical wave-guide optically connecting the first micro tile element and the second micro tile element with each other, wherein the optical wave-guide is in contact with and covers the first and second micro tile elements such that at least the light emitting part of the first micro tile element and at least the light receiving part of the second micro tile element are covered. Applicant respectfully submits that such an optical interconnection circuit is not taught or suggested by Yoshimura 736.

Yoshimura 736 describes an optical circuit system which takes out at least a portion of the light of a light power source corresponding to at least one type of output voltage of an IC, board, multichip module, electronic element, or opto-electronic element and produces an optical signal, wherein the light power source is an optical wave-guide into which light has

been introduced. Light reflecting portions are provided at its ends and/or middle. A signal transmission wave-guide is formed in contact with the side surface and/or top or bottom surface of the optical wave-guide or in proximity to the same at a certain distance, and the optical signal corresponding to at least one type of output voltage of the IC, board, multichip module, electronic element, or opto-electronic element is made to propagate to the signal transmission wave-guide. See the Abstract.

In Yoshimura 736, then, the optical wave-guide is described to be provided on or in a substrate, and an optical element is provided on the optical wave-guide or at the same level as the optical wave-guide. For example, Yoshimura 736 describes that the optical wave-guide is embedded in the substrate while the optical element (LD) is provided on the substrate. See Figure 43 of Yoshimura 736.

Thus, contrary to the structure of the optical interconnection circuit recited in claim 1, Yoshimura 736 fails to teach or suggest an optical wave-guide that covers first and second micro tile elements such that at least the light emitting part of the first micro tile element and at least the light receiving part of the second micro tile element are covered. In no embodiments described in Yoshimura 736 is the optical wave-guide provided to cover the optical elements in this manner. Accordingly, Yoshimura 736 completely fails to teach or suggest claim 1 of the present application.

For at least the foregoing reasons, Applicant submits that Yoshimura 736 neither anticipates nor renders obvious the optical interconnection circuit of claim 1 or claims dependent therefrom. Reconsideration and withdrawal of the rejections are thus respectfully requested.

II. Rejections Relying Upon Yoshimura 845

Claims 1-7, 12, 13 and 19-20 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,690,845 (Yoshimura 845). In addition, claims 8-11

and 14-18 were rejected under 35 U.S.C. §103(a) relying upon Yoshimura 845. These rejections are respectfully traversed.

Yoshimura 845 describes a three-dimensional opto-electronic module having a plurality of opto-electronic (O/E) layers, with optical signals being routed between O/E layers within one or more three-dimensional volumes. In preferred embodiments, the O/E layers are disposed over and above one another with at least one of their edges aligned to one another. At least two of the O/E layers have wave-guides with ends near the aligned edges. A plurality of Z-connector arrays are disposed between the O/E layers and within the three-dimensional volumes to provide a plurality of Z-direction wave-guides. A first vertical optical coupler couples light from one wave-guide in one O/E layer to a Z-direction wave-guide, and a second vertical optical coupler couples the light from the Z-direction wave-guide to a second wave-guide in a second O/E layer. In further preferred embodiments, segments of the Z-connector arrays are held by a holding unit. See the Abstract.

Figures 33-37 of Yoshimura 845 illustrate embodiments in which IC chips are encapsulated in a dielectric film with contact pads formed on the film surface for attachment to an active substrate. This enables the stacking of the alternating IC chip layers and active substrate layers to form a three-dimensional multichip module with both electrical and optical interconnects. In these embodiments, a VCSEL emitter device 336 and a photo-detector device 328 are included in an active substrate 320. The VCSEL emitter device 336 transmits an optical signal to a wave-guide 324a above the emitter device 336. Wave-guide 324a conveys the signal to a photo-detector device 328.

The structure described in Yoshimura 845 differs from, and fails to teach or suggest, the structure recited in claim 1. In particular, in claim 1, the wave-guide is required to be in contact with and cover the first and second micro tile elements such that at least the light emitting part of the first micro tile element and at least the light receiving part of the second

micro tile element are covered. While Yoshimura 845 illustrates a wave-guide over light emitting and light receiving elements, Yoshimura 845 nowhere teaches or suggests that the wave-guide must also be in contact with and cover the light emitting and light receiving parts of each of the elements. In fact, by specifically teaching a separation of the wave-guide from the elements and the use of couplers to transfer between the elements and the wave-guide, Yoshimura 845 teaches one of ordinary skill in the art away from the optical interconnection circuit of claim 1.

For at least the foregoing reasons, Applicant submits that Yoshimura 845 neither anticipates nor renders obvious the optical interconnection circuit of claim 1 or claims dependent therefrom. Reconsideration and withdrawal of the rejections are thus respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-20 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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